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Schematic-Driven IC Layout Editor Accelerates SoC Design

Hybrid Approach Can Bring 300 Percent Performance Gains

ASICs Join Full-custom Flow

By Richard C. Smith

The ASIC design methodology -- using HDLs, synthesis, place-and-route, and timing analysis -- has provided the world with countless ICs in applications from set-top boxes to mobile communications. Had full-custom design approaches been required for these circuits, there would not have been enough designer hours available to create even a fraction of them.

In the last few years, ASIC technologies have provided ever-greater capability to design more complex chips. But little has been done to push the limits of speed and power.

As process technologies shrink from 0.25 to 0.18 micron and smaller geometries, the wiring begins to dominate the delay computation. For these designs, the time spent adjusting the HDL trying to achieve an acceptable level of performance soon exceeds the time it would take for a full-custom design.

Some new, fully automated approaches promise 10 to 30 percent performance improvements over standard ASIC design methods. Yet these improvements mean nothing when improvement of at least 100 percent is required just to meet the new clock rates for some applications, such as networking and graphics chips.

Rather than pushing ASIC methodologies to provide higher performance, designers can apply a hybrid approach by incorporating selected ASIC design techniques in a full-custom IC design flow.

The ASIC techniques reduce design effort while maintaining performance at the full-custom level. The selected ASIC techniques would include the use of standard-cell libraries, accurate wiring estimates and timing analysis.

Full-custom methodologies are distinguished by the ability to control the design from the architecture down to the cell level, full control over cell placement and complete knowledge of each critical path in the design. Data path-based designs allow immediate, visual understanding of timing for even the largest and most complex circuitry, allowing designers to identify problems and apply corrections directly and deterministically. Micro Magic has adopted this hybrid methodology in its design services with astounding results.

In the Micro Magic design methodology, ASIC design methods are used for general control logic and noncritical portions of processor design. The data path methodology is used on performance-critical portions. It requires only slightly more effort than the first pass through a standard ASIC flow, while keeping performance near that of full-custom. Rather than limiting design options, this methodology supports the inclusion of control logic, clock trees, scan, built-in self-test and custom blocks.

Using this hybrid method, the Micro Magic design services team has consistently achieved performance im-provements of more than 300 percent compared with standard ASIC design methods. Moreover, these data-path-based designs are about 40 percent smaller than standard ASICs and use an average of 10 percent less power. One recent example is a 220-MHz network processor that achieved only 65 MHz using standard ASIC design methods. Another is a recently completed, very large DSP data path core for Malleable Technologies that met timing on the very first pass.

Is the ASIC design methodology dying? Absolutely not. About 80 percent of a typical processor design is well outside the critical path and can be completed using standard ASIC methodologies to achieve the shorter design cycles with minimal effort. The remaining 20 percent of the typical processor design must be addressed with new methodologies.

The ASIC approach relies on adjusting the HDL in hopes that, after long design iterations, an improved result is achieved when the final timing analysis is run. Starting from the full-custom approach and finding ways to reduce effort has proved to be a tremendously beneficial approach for designers at Micro Magic.

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